Motivation

- Hardware platforms for NN Accelerators:
  - CPU
  - GPU
  - FPGA
  - ASIC

  Case of programmability vs Efficiency

  - FPGAs are reconfigurable
    - can exploit different types of NNs
    - can adapt to evolving NN implementations

- Problem
  - FPGAs are not easy to use:
    - Require hardware design expertise
    - Require use of low level hardware language
    - Steep learning curve for tools
    - Workflow is not portable

- Existing solutions
  - OpenCL
    - Outperformed by hand-written HDL
  - High-level tools provided by vendors (e.g. Xilinx SDAccel)
    - Not as flexible as HDL
    - May not support upcoming NN architectures
  - HDL generation based on pre-built RTL components
    - Not flexible enough

- The Lift approach
  - Specify behaviour in a high-level functional language
  - Optimise using rewrite rules
    - On algorithmic level &
    - On hardware-specific level
  - Generate hardware implementation
  - Estimate design quality using a performance model
    - Feedback results into new design generation

Advantages

- Target CPU, GPU and FPGAs
- Support arbitrary NN architectures
- Portable across many FPGAs
- Automatically optimised